REMARKS

Claims 1, 3, 9, 30-32, 34, 35, 37, 40, 42, and 44 are rejected as being anticipated under 35 U.S.C. 102(e) by Rhee, *et al.* (United States Patent Number 6,774,712). Claims 39, 41 and 43 are deemed to be inherent since, according to the Office Action at page 5, third paragraph, the claimed structure is anticipated by Rhee, *et al.* Applicants therefore assume that claims 39, 41 and 43 are likewise rejected under 35 U.S.C. 102(e) by Rhee, *et al.* Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Sher (United States Patent Number 6,633,196). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Bae, *et al.* (United States Patent Number 6,373,754). Claims 33, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhee, *et al.* in view of Park, *et al.* (United States Patent Number 5,349,559). Claims 10-12, 14-17, 23, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (United States Publication Number 2002/0053943) in view of Sher. In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the cited references. Accordingly, reconsideration of the rejections is respectfully requested.

With regard to the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* in view of Sher, and with regard to the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Bae, *et al.*, and with regard to the rejections of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.*, the Office Action continues to cite Rhee, *et al.* as a prior art reference in the abovementioned 35 U.S.C. 103(a) rejections, despite Applicant's submission in Amendment After Final Rejection filed on October 10, 2007 that Rhee, *et al.* is disqualified as a prior art reference to the present application, pursuant to 35 U.S.C. 103(c), and in which the Applicants provided a Statement Concerning Common Ownership to affirm that Rhee, *et al.* was subject to an obligation of assignment to the same entity, Samsung Electronics Co., Ltd., as the present application at the time the present invention was made.

Specifically, since Rhee, *et al.* is prior art under 35 U.S.C. 102(e), and since Rhee, *et al.*

was subject to an obligation of assignment to the same entity, i.e. Samsung Electronics Co., Ltd., as the present application at the time the present application was made, it follows that, with regard to the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* in view of Sher, and with regard to the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Bae, *et al.*, and with regard to the rejections of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.*, Rhee, *et al.* is disqualified as a prior art reference to the present application, pursuant to 35 U.S.C. 103(c). Support for Applicants' submission of Rhee's disqualification as a prior art reference pursuant to 35 U.S.C. 103(c) is provided in the Manual of Patent Examining Procedure (M.P.E.P.) at least at section 706.02(l).

Accordingly, reconsideration and removal of the rejections of claims 7 and 8 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Sher are respectfully requested.

If a rejection under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Sher is maintained, the Examiner is requested to explain specifically why Rhee, *et al.* is available as a reference.

In addition, reconsideration and removal of the rejection of claim 2 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Bae, *et al.* are respectfully requested.

If a rejection under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Bae, *et al.* is maintained, the Examiner is requested to explain specifically why Rhee, *et al.* is available as a reference.

In addition, reconsideration and removal of the rejections of claims 33, 36, and 38 under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.* are respectfully requested.

If a rejection under 35 U.S.C. 103(a) based on the combination of Rhee, *et al.* and Park, *et al.* is maintained, the Examiner is requested to explain specifically why Rhee, *et al.* is available as a reference.

Further, none of the remaining references (Sher, Bae, *et al.*, Park, *et al.*) support a substitute rejection of any of the claims 2, 7, 8, 33, 36, and/or 38 based on lack of novelty (35 U.S.C. §102) or based on obviousness (35 U.S.C. §103). Applicants have reviewed the Sher, Bae, *et al.*, and Park, *et al.* references and have found no teachings in any of these references that would support a substitute rejection.

Independent claims 1 and 34 are amended herein to clarify that a semiconductor device comprises a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device.

With regard to the rejections of claims 1, 3, 9, 30-32, 34, 35, 37, 40, 42, and 44 under 35 U.S.C. 102(e) based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a semiconductor device comprising a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 34.

The Office Action at least at pages 2, 3, 5, and 12 refers to a complementary control signal PDPDEB of Rhee, *et al.* as being analogous to a control signal, as claimed in claims 1 and 34, and further refers to a control signal PDPDE of Rhee, *et al.* as being analogous to an input signal. However, there is no teaching or suggestion in Rhee, *et al.* of a control signal generating circuit that receives the control signal PDPDE and generates the complementary control signal

PDPDEB responsive to the control signal PDPDE. Instead of being responsive to the control signal PDPDE (referred to in the Office Action as an input signal), the complementary control signal PDPDEB of Rhee, *et al.* is responsive to a control command input from either outside the chip of Rhee, *et al.* or by a transition of a voltage level at a specific pin of the chip of Rhee, *et al.* (see Rhee, *et al.,* column 3, lines 18-20).

Further, there is no teaching or suggestion in Rhee, *et al.* of the control signal PDPDE (referred to in the Office Action at page 3, line 1 as an input signal) being an input signal that is provided to a control signal generating circuit, and that is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34.

The Office Action at page 2 section 4 refers to Rhee, *et al.* as disclosing a control signal generating circuit outputting a PDPDEB signal. However, while Rhee, *et al.* further teaches that the PDPDEB signal is output to transistors 32, 40, and 42 of Rhee, *et al.* (see Rhee, *et al.*, Figure 1) or output to transistors 42 and 58 (see Rhee, *et al.*, Figure 4), Applicants find no teaching or suggestion in Rhee, *et al.* of a control signal generating circuit that generates the PDPDEB signal. Even if Rhee, *et al.* arguably teaches a control signal generating circuit that generates the PDPDEB signal, as described herein, there is no teaching or suggestion in Rhee, *et al.* of a control signal generating circuit that receives an input signal and generates a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 34.

The Office Action at page 12 further refers to signal PDPDEB of Rhee, *et al.* (referred to in the Office Action as a control signal) as being simultaneously input into transistors 58 and 42 of Rhee, *et al.* at the same time that signal PDPDE (referred to in the Office Action as an input signal) is simultaneously input into transistors 60, 68, and 50 of Rhee, *et al.* (see Rhee, *et al.*, Figure 4). However, this description in the Office Action is different than the present invention. Specifically, there is no teaching or suggestion in Rhee, *et al.* of an input signal that is provided to a control signal generating circuit, and that is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34. Even though signal PDPDE of Rhee, *et al.* is output to the gate of PMOS transistor 68, which is coupled between a voltage source and an internal circuit 56, and further output to the gate of PMOS transistor 60, which is coupled between a voltage source and the output of an amplifier 52, and further output to the gate of NMOS transistor 50, which is coupled between NMOS transistor 48 and ground, there is no relationship between the three abovementioned elements of Rhee, *et al.* receiving the signal PDPDE of Rhee, *et al.* (referred to in Rhee, *et al.* as an input signal) and a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34. Instead, the Office Action refers to the signal PDPDE of Rhee, *et al.* being simultaneously output to multiple elements (gate of transistor 68, etc.), and further refers to as signal PDPDEB of Rhee, *et al.* being simultaneously output to multiple elements (gate of transistor 42, etc.), but the Office Action does not explain why Rhee, *et al.* teaches or suggests that the signal PDPDE of Rhee, *et al.* (referred to in the Office Action as an input signal) is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34. In particular, the signal PDPDE of Rhee, *et al.* simultaneously output to multiple transistors is different from an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 1 and 34.

Along these lines, it is further submitted that Rhee, *et al.* fails to teach or suggest that the control signal PDPDEB (referred to in the Office Action as a control signal) is a control

signal that is activated when the control signal PDPDE (referred to in the Office Action as an input signal) indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 1 and 34.

The Office Action at page 12, third paragraph, refers to Rhee, *et al.* as teaching at least two bits being put into a semiconductor device because at least one bit is input into transistor 42 and at least one bit is input into transistor 58 of Rhee, *et al.* The Office Action, however, does not distinguish between a number of data bits and a predetermined number of bits, as claimed in claims 1 and 34. Specifically, while the Office Action refers to Rhee, *et al.* as teaching at least two bits, the Office Action does not specify whether the at least two bits of Rhee, *et al.* are predetermined bits or data bits. If the Office Action refers to the at least two bits of Rhee, *et al.* as being analogous to a predetermined number of bits, one of skill in the art understands that, in order for the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device to be more than a predetermined number of bits greater than one bit (according the Office Action, at least two bits), then the number of data bits must be three (3) or more data bits. There is no such teaching or suggestion in Rhee, *et al.* of a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device to be more than a predetermined number of bits, which is greater than one bit, as claimed in claims 1 and 34.

On the other hand, if the Office Action refers to the at least two bits of Rhee, *et al.* as being analogous to a number of data bits, then there is no analog in Rhee, et al. to a predetermined number of bits being greater than one bit, as claimed in claims 1 and 34.

Further, with regard to statements made in the Office Action at page 12, third paragraph, even if at least two bits are put into a semiconductor device because at least one bit is

input into transistor 42 and at least one bit is input into transistor 58 of Rhee, *et al.*, the Office Action refers to the signal PDPDEB input into transistors 42 and 58 as being a control signal, not an input signal. Thus, it is irrelevant whether multiple bits are input into transistor 42 and/or transistor 58 of Rhee, *et al.* As described above, there is no explanation in the Office Action as to the PDPDEB signal being a control signal that is responsive to an input signal related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in claims 1 and 34.

The Office Action at page 13 further refers to a circuit being activated during two consecutive bits in a first mode. However, two consecutive bits are different than a number of data bits being simultaneously input to or output from a semiconductor device, as claimed.

With regard to the rejections of independent claims 35 and 37 based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a control signal generating circuit for generating a control signal according to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in amended independent claims 35 and 37, for reasons similar to those described above with regard to independent claims 1 and 34.

In addition, with regard to independent claims 34 and 37 based on Rhee, *et al.*, it is submitted that Rhee, *et al.* fails to teach or suggest a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal when the control signal is inactivated, wherein the comparing circuit includes a comparator connected between the external power voltage and a first node and comparing the reference voltage to the internal voltage to generate the driving signal, and a switching circuit connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claims 34 and 37.

Applicants pointed out the differences between the present invention as claimed in claims 34 and 37 and Rhee, *et al.* by way of example in Amendment After Final Rejection filed on October 10, 2007. Specifically, as shown in Figure 3 of the drawings as filed, a comparing

circuit includes a comparator 10 that is connected between the external power voltage EVC and a first node and compares a reference voltage VREF to an internal voltage IVC to generate a driving signal, and a switching circuit N2 connected between the first node and a ground voltage and cutting off a ground voltage supplied to the comparator 10 when C control signal C is activated, as claimed in independent claim 37. There is no such teaching or suggestion in Rhee, *et al.* of this claimed feature. Specifically, there is no teaching or suggestion in Rhee, *et al.* of a switching circuit connected between a first node and a ground voltage and cutting off the ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claims 34 and 37. Assuming arguably that the signal PDPDEB signal of Rhee, *et al.* is a control signal, the PDPDEB signal of Rhee, *et al.* is applied to transistors 32, 40, and 42 (Figure 1 of Rhee, *et al.*) and transistors 42 and 58 (Figure 4 of Rhee, *et al.*). However, none of the abovementioned transistors of Rhee, et al. is a switching circuit connected between a first node and a ground voltage that cuts off a ground voltage supplied to amplifiers 30, 52, or 54 shown in Figures 1 and 4 of Rhee, *et al.* when the PDPDEB signal is activated.

The Office Action at page 5 refers to claims 34 and 37 as being rejected for similar reasons as reasons previously described in the Office Action. However, nowhere in the Office Action is there any explanation as to why Rhee, et al. teaches or suggests a switching circuit connected between a first node and a ground voltage and cutting off the ground voltage supplied to the comparator when the control signal is activated, as claimed in independent claims 34 and 37.

With regard to the rejection of claim 9 under 35 U.S.C. 102(e) based on Rhee, *et al.*, the Office Action at page 4 maintains the rejection of claim 9 in the same manner as in the previous Office Action dated August 10, 2007, that is, an input signal is not a structural component, etc. However, the current Office Action does not address the limitation of claim 9 as amended in the Amendment After Final Rejection filed on October 10, 2007. Specifically, Applicants assert that a control signal generating circuit comprises a mode setting circuit that sets a mode of the semiconductor device, and generates the control signal in response to the input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits, as claimed in

claim 9, is a structural component of the present invention.

Accordingly, it is submitted that, with regard to claim 9, there is no teaching or suggestion in Rhee, et al. of a signal generating circuit comprising a mode setting circuit that sets a mode of the semiconductor device, and generating a control signal in response to an input signal, wherein the input signal is a mode setting signal comprising a plurality of mode setting bits, as claimed in claim 9.

With regard to the rejections of claims 30-32 based on Rhee, *et al.*, the Office Action at page 4 maintains the rejection of claims 30-32 in the same manner as in the previous Office Action dated August 10, 2007, that is, claims 30-32 are deemed to be intended use. However, the current Office Action does not address the limitation of claims 30-32 as amended in the Amendment After Final Rejection filed on October 10, 2007. Specifically, Applicants assert that a mode setting circuit produces a value that is represented by mode setting bits and a mode setting command, wherein a control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by a semiconductor device. Accordingly, it is submitted that Rhee, *et al.* fails to teach or suggest a mode setting circuit that produces a value that is represented by mode setting bits and a mode setting command, wherein a control signal generating circuit generates the control signal in response to the value, the value of the mode setting bits corresponding to the number of bits being processed by a semiconductor device, as claimed in claims . With regard to statements made in the Office Action at page 4, Applicants submit that amended claims 30-32 are not statements of intended use, but, rather, are limitations that recite a structural component of the present invention, i.e., a mode setting circuit.

For at least the reasons described herein, it is submitted that Rhee, *et al.* fails to teach or suggest the invention set forth in the amended claims. Reconsideration and removal of the rejections of claims 1, 3, 9, 30-32, 34, 35, 37 and 39-44 under 35 U.S.C. 102(e) based on Rhee, *et al.* are respectfully requested.

With regard to the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C.

103(a) based on the combination of Yamasaki, *et al.* and Sher, it is submitted that neither Yamasaki, *et al.* nor Sher teaches or suggests a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23.

Yamasaki, *et al.* teaches a test mode setting circuit 3 that receives signals /RAS, /CAS, /WE, and Add (referred to in the Office Action as an input signal), and activates/deactivates a test mode designating signal TE (referred to in the Office Action as a control signal) when the signals are set to a predetermined combination of states (see Yamasaki, *et al.*, Figure 5A and page 7, paragraph [0092]). However, there is no teaching or suggestion in Yamasaki, *et al.* of the /RAS, /CAS, /WE, and Add signals being an input signal related to a number of data bits that are simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in independent claims 10 and 23. Further, there is no teaching or suggestion in Yamasaki, *et al.* of a predetermined number of bits being greater than one bit, as claimed in independent claims 10 and 23. Thus, it follows that Yamasaki, et al. does not teach or suggest a predetermined number of bits that is compared to a number of data bits simultaneously input to a semiconductor device or output from the semiconductor device to determine whether a control signal is activated or inactivated. Specifically, it is submitted that, since Yamasaki, *et al.* fails to teach or suggest either an input signal related to a number of data bits that are simultaneously input to the semiconductor device or output from the semiconductor device, as claimed in

independent claims 10 and 23, or a predetermined number of bits, as claimed in independent claims 10 and 23, it follows that Yamasaki, *et al.* further fails to teach or suggest that an control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, and that the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23.

Sher teaches a device that includes programmable circuits coupled to an external communication terminal such as a bond pad and to one of many load circuits such as input buffers, wherein the programmable circuits are configurable to load the terminal with one or more of the load circuits and to isolate the terminal from the rest of the load circuits (see Sher Summary of the Invention). The device of Sher includes an inventive IC die 10 comprising load circuits 12 and 14 capable of communicating with external circuitry (not shown) through programmable circuits 16 and 18 and a terminal in the IC die 10, such as a bond pad 20 (see Sher, Figure 1). However, there is no teaching or suggestion in Sher of a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23.

In addition, it is submitted that Yamasaki, *et al.* and Sher fail to teach or suggest an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23.

In particular, the Office Action at page 7 refers to Yamasaki, *et al.* as teaching an internal voltage generating circuit being coupled to the test mode setting circuit of Figure 5a of Yamasaki, *et al.* (referred to in the Office Action as a control signal generating circuit), and receiving a control signal TE. The test mode setting circuit of Figure 5a of Yamasaki, *et al.* outputs control signal TE to transfer gates 2c and 2e of driving circuit 2, and further outputs control signal TE to transistor 2f coupled to differential amplifier 2b (see Yamasaki, *et al.*, Figure 1). Thus, while the test mode setting circuit of Figure 5a of Yamasaki, *et al.* is coupled to various components of driving circuit 2, which generates a reference voltage Vrfo (see Yamasaki, *et al.*, Figure 1), there is no teaching or suggestion of the test mode setting circuit of Figure 5a of Yamasaki, *et al.* being coupled to the voltage down converter VDC of Yamasaki, *et al.*, which generates an internal power supply voltage intVcc.

Sher teaches an integrated circuit die 10 that includes load circuits 12 and 14, circuits 16 and 18, and a terminal in the IC die 10, such as a bond pad 20 (see Sher, Figure 1). However, Sher likewise fails to teach or suggest an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23.

Further, there is no teaching or suggestion in Yamasaki, *et al.* and Sher of an nternal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the

reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

Yamasaki, *et al.* fails to teach or suggest that the abovementioned driving circuit 2 of Yamasaki, *et al.* is an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23. Specifically, there is no teaching or suggestion in Yamasaki, *et al.* of reference voltage Vrfo generated by driving circuit 2 being an internal voltage generated by an internal voltage generating circuit, as claimed in claim 10, or making the internal voltage have the reference voltage level in response to a driving signal, as claimed in claim 23. One of skill in the art readily understands that an internal voltage is generated for a memory cell array, a peripheral circuit, or a delay locked loop (see, for example, pages 1-2 and paragraph [0004] of the specification as filed). However, in Yamasaki, *et al.*, reference voltage Vrfo is transmitted to a pad 1 (see Yamasaki, *et al.*, Figure 1 and page 5, paragraph [0068], lines 1-6), and therefore, the reference voltage Vrfo of Yamasaki, *et al.* is different than the internal voltage IVC as claimed in claims 10 and 23.

With regard to Sher, there is no teaching or suggestion in Sher of an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim

23.

Accordingly, it is submitted that Yamasaki, *et al.* and Sher, taken alone or in combination, fail to teach or suggest the invention set forth in amended independent claims 10 and 23. Specifically, neither Yamasaki, *et al.* nor Sher teaches or suggests a semiconductor device comprising a control signal generating circuit receiving an input signal and generating a control signal responsive to the input signal, wherein the input signal provided to the control signal generating circuit is related to a number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device, wherein the control signal is activated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is more than a predetermined number of bits, the predetermined number of bits being greater than one bit, and the control signal is inactivated when the input signal indicates that the number of data bits being simultaneously input to the semiconductor device or output from the semiconductor device is less than the predetermined number of bits, as claimed in amended independent claims 10 and 23, or an internal voltage generating circuit coupled to the control signal generating circuit for receiving the control signal, as claimed in amended independent claims 10 and 23, or an internal voltage generating circuit comprising a comparing circuit for comparing a reference voltage to an internal voltage to generate a driving signal, and further comprising an internal voltage driving circuit for receiving an external power voltage and generating the internal voltage in response to the driving signal, as claimed in claim 10, or an internal voltage generating circuit comparing a reference voltage to an internal voltage to make the internal voltage have the reference voltage level in response to a driving signal when the control signal is inactivated, as claimed in claim 23.

Since neither Yamasaki, *et al.* nor Sher teaches or suggests these claimed features, there is no way to combine the references to obtain teaching or suggestion of the claimed features, and therefore, there is no combination of the references that teaches or suggests the invention set

forth in the amended claims.

Since the combination of Yamasaki, *et al.* and Sher fails to teach or suggest the invention set forth in the claims, the claims are believed to be allowable over the cited references. Accordingly, reconsideration and removal of the rejection of claims 10-12, 14-17, 23, 25, and 27-29 under 35 U.S.C. 103(a) based on the combination of Yamasaki, *et al.* and Sher are respectfully requested.

In view of the amended claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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